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Claims

[c1] 1. A method of fabricating a flip chip package, comprising the steps of:
providing a substrate;
connecting a chip to the substrate, wherein the chip comprises an active surface and a corresponding backside and the active surface comprises a plurality of bumps such that the chip and the substrate are electrically connected through the bumps;
attaching a heat sink to the backside of the chip, wherein the heat sink comprises at least a through hole located outside a perimeter of the chip;
performing a dispensing process via the through hole by injecting an underfill material into a space between the active surface of the chip and the substrate; and
curing the underfill material to fix the substrate and the chip.

[c2] 2. The method of claim 1, wherein the dispensing process comprises passing a dispensing needle through the through hole to deliver the underfill material to the space between the chip and the substrate as well as the heat sink.

[c3] 3. The method of claim 1, wherein the through hole is positioned outside the perimeterof the chip and adjacent to the chip.

[c4] 4. The method of claim 1, wherein the heat sink has a coefficient of thermal expansion comparable to the substrate.

[c5] 5. The method of claim 1, wherein the heat sink comprises an upper surface and a lower surface, and wherein the lower surface further comprises at least a stopper on an outer edge of the through hole.

[c6] 6. The method of claim 1, wherein before the step of attaching the heat sink to the chip, further comprises applying a thermal conductive layer to the backside of the chip.

[c7] 7. The method of claim 1, wherein the underfill material comprises epoxy resin.

[c8] 8. The method of claim 7, wherein the epoxy resin comprises a thermal-setting epoxy resin.

[c9] 9. The method of claim 1, wherein the step of performing the dispensing process further comprises injecting the underfill to cover a portion of the heat sink to connect the substrate and the heat sink.

[c10] 10. A flip chip package structure, comprising:
a chip having an active surface and a corresponding backside, wherein the active surface comprises a plurality of bumps thereon;
a substrate, wherein the substrate is connected to the active surface of the chip through the bumps;
a heat sink attached to the backside of the chip, wherein the heat sink comprises at least a through hole located outside a perimeter of the chip; and
an underfill material that fills up a space between the active surface of the chip and the substrate and connects the heat sink and the substrate.

[c11] 11. The flip chip package structure of claim 10, wherein the through hole is positioned outside the perimeter and adjacent to the chip.

[c12] 12. The flip chip package structure of claim 10, wherein the heat sink has a coefficient of thermal expansion comparable to the substrate.

[c13] 13. The flip chip package structure of claim 10, wherein the heat sink has an upper surface and a lower surface, and wherein the lower surface further comprises at least a stopper on an outer edge of the through hole.

[c14] 14. The flip chip package structure of claim 10, further

comprising a thermal conductive layer between the backside of the chip and the heat sink.

[c15] 15. The flip chip package structure of claim 10, wherein the underfill material comprises an epoxy resin.

[c16] 16. The flip chip package structure of claim 15, wherein the epoxy resin comprises a thermal-setting epoxy resin.

[c17] 17. The flip chip package structure of claim 13, wherein the stopper is downward protruded from the lower surface of the heat sink.

[c18] 18. The flip chip package structure of claim 13, wherein the stopper is located outside the perimeter of the chip.

[c19] 19. The flip chip package structure of claim 10, further comprising a stiffener connecting the substrate and the heat sink.

[c20] 20. The flip chip package structure of claim 10, wherein the underfill material fills the through hole.

[c21] 21. The flip chip package structure of claim 10, wherein the heat sink contacts with the substrate.